IN THE SPECIFICATION

Please replace paragraphs [1032], [1074] and [1085] in the Specification with the following rewritten paragraphs:

[1032] FIG. 3 shows an embodiment of adaptive PFD 210, which includes a PFD 310, a scaling unit 340, and a control circuit 350. Within PFD 310, the reference signal and the feedback signal are provided to the clock inputs of D flip-flops (DFFs) 312a and 312b, respectively. The data (D) inputs of DFFs 312a and 312b couple to the power supply and receive logic high. The $\overline{Q}$ outputs of DFFs 312a and 312b provide the S1 and S2 signals, respectively. An inverter 314a receives and inverts the S1 signal and provides an S1b signal to the data input of a latch 316a and the clock input of a latch 316b. An inverter 314b receives and inverts the S2 signal and provides an S2b signal to the data input of latch 316b and the clock input of latch 316a. Latches 316a and 316b are thus cross-coupled by the S1b and S2b signals. The Q output of latch ~~316aprovides~~ 316a provides an INC signal, and the Q output of latch ~~316bprovides~~ 316b provides a DEC signal.

[1074] Current sources 912a through 912l in section 910 and current sources ~~934a~~ 932a through ~~934p~~ 932p in section 930 may be implemented with cascode P-channel metal oxide semiconductor (P-MOS) current sources. Cascade P-MOS current sources can enhance iDAC linearity and provide good immunity to low frequency supply noise.

[1085] DSP 1220 includes various processing units such as, for example, a multiply-accumulate (MACC) unit 1222, an arithmetic logic unit (ALU) 1224, an internal controller 1226, a processor 1228, a memory unit 1230, and a bus control unit 1232, all of which are coupled via a bus 1236. DSP 1220 further includes a digital PLL 1234 that may be implemented with digital PLL 200. Digital PLL 1234 receives a reference signal (e.g., from a temperature compensated crystal oscillator (TCXO)) and generates clock signals for the processing units within DSP 1220 and possibly processing units external to DSP 1220 (e.g., a main controller 1240 and a main memory unit 1242). DSP 1220 may perform encoding, interleaving, modulation, channelization (e.g., with Walsh codes), spectral spreading ~~spread~~, and so on, for the transmit path. DSP 1220 may perform despreading, channelization,

demodulating, deinterleaving, decoding, and so on, for the receive path. The processing by DSP 1220 is determined by the communication system.